AF 2835

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Art Unit: 2835
Examiner: M. Datskovsky

In Re PATENT APPLICATION Of:

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| Applicant: | Seiji ANDOH | ) |
| Serial No.: | 09/376,063 | ) |
| Filed: | August 17, 1999 | ) **RESUBMISSION OF APPEAL BRIEF WITH CORRECTION** |
| For: | PACKAGE STRUCTURE FOR A SEMICONDUCTOR DEVICE | ) |
| Attorney Ref: | OKI 226 | ) |

**Mail Stop Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

An Appeal Brief was originally submitted on April 23, 2004 in support of the Notice of Appeal filed in this matter on February 23, 2004. On May 21, 2004, the Office issued a notice indicating that the Appeal Brief was not acceptable because the statement of the issues was missing, and giving the Applicant a period of one month to supply the omitted material.

A corrected Appeal Brief, including the missing section identified by the Office (see page 5 of the corrected Appeal Brief) is submitted herewith. The Appeal Brief is otherwise unchanged from the original version.

The omission having been corrected, consideration of the Appeal Brief on its merits is respectfully requested.

Respectfully submitted,

Date: June 9, 2004

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Enclosure: Appeal Brief (Corrected)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In Re PATENT APPLICATION Of:

| | | |
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| Applicant: | Seiji ANDOH | ) |
| Serial No.: | 09/376,063 | ) |
| Filed: | August 17, 1999 | ) |
| For: | PACKAGE STRUCTURE FOR A SEMICONDUCTOR DEVICE | ) **APPEAL BRIEF (CORRECTED)** |
| Art Unit: | 2835 | ) |
| Examiner: | M. Datskovsky | ) |
| Attorney Ref: | OKI 226 | ) |

June 9, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed February 23, 2004. This Appeal Brief was originally filed on April 23, 2004, and is being timely resubmitted with corrections in response to the Office communication regarding this matter mailed May 21, 2004.

FEE ENCLOSED:$0
Please charge any further fee to our Deposit Account No. 18-0002

## I. REAL PARTY IN INTEREST

Oki Electric Industry Co., Ltd.

## II. RELATED APPEALS AND INTERFERENCES

NONE

## III. STATUS OF CLAIMS

Claims 20, 22, 24-29 and 31 are pending. Each of claims 20, 22, 24-29 and 31 is under appeal.

## IV. STATUS OF AMENDMENTS

Amendments were filed in this application on July 20, 2000, December 11, 2000, June 5, 2001, November 26, 2001, May 13, 2002, August 26, 2002 and March 6, 2003. All of these previously filed amendments have been entered.

## V. SUMMARY OF THE INVENTION

The present invention is directed to a package structure for a semiconductor device that has radiation solder bumps and connection solder bumps on the back surface for surface mounting the semiconductor device to a printed circuit board. The inventive semiconductor device, as recited in claim 20 and with reference to Figures 1 and 2 of the application, includes:

- a substrate 11a having a main surface and a back surface, the back surface having a central area, a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding the intermediate area;
- a semiconductor chip disposed on the main surface;
- a first bump unit 13 disposed in the central area of the back surface; and
- a second bump unit 14 disposed in the peripheral area of the back surface.

The first bump unit located in the central area of the substrate 11a includes a plurality of bumps that are spaced a first distance apart from each other and radiate heat from the semiconductor device to the surface to which the device is mounted (see, for example, page 4, lines 20-21). The second bump unit includes a plurality of bumps that are spaced a second distance apart from each other, the second distance being greater than the first distance between the bumps in first bump unit, and the second bump unit transmits signals to and from the semiconductor device to the printed circuit board to which it is mounted (see, for example, page 4, lines 21-26). In the first bump unit, bumps are spaced close together to achieve an improved coefficient of thermal conductivity between the semiconductor device and the surface on which it is mounted (see, for example, page 5, lines 16-22). Because the first unit of bumps carry no electrical signals, there is no concern that solder bridges may form between the closely spaced bumps of the first bump unit when the bumps are reflowed during the process of surface mounting the semiconductor device. On the other hand, the bumps of the second bump unit carry signals to and from the semiconductor device and are spaced further apart than those in the first bump unit so that short-circuits caused by solder bridges between the bumps of the second bump unit, formed during the mounting process, will not occur (see, for example, page 5, lines 10-15). For example, the diameter of the radiation bumps 13 and connection bumps 14 is 0.75 mm, the distance between the radiation bumps 13 is 1.00 mm and the distance between the connection bumps is 1.27 mm (page 5, lines 23-26). Preferably, the plurality of bumps included in the first bump unit and the second bump unit are spherical in shape.

In the present invention as claimed, the second distance (i.e., the distance between the connection bumps 14) is less than a third distance between the central area and the peripheral area on the back surface of the substrate 11a. In other words, as recited in claim 22, the width of

the intermediate area between the central area and the peripheral area, is greater than the second distance.

To assure an adequate number individual signal connections for the semiconductor device, the plurality of bumps included in the second bump unit is preferably greater in quantity than the plurality of bumps included in the first bump unit (see, for example, page 4, lines 23-26).

In another aspect of the invention, as recited in claims 26 and 28, and with reference to Figures 3 and 4 of the application, the plurality of connection bumps 14 are spaced at a distance sufficient to assure that when heat treatment is applied causing the bumps of the first and second bump units to melt, the connection bumps 14 remain apart from each other and make individual connections to the connection pads 22 on the printed circuit board 20 (see, for example, page 5, lines 10-15). On the other hand, the radiation bumps 13 are sufficiently close to each other that upon application of the heat treatment to the device, they melt and become fused to each other as a unitary body 30 in contact with the radiation pads 21 on the printed circuit board 20 (see, for example, page 5, lines 16-22). As recited in claim 31, the distance between the radiation bumps 13 in the first bump unit is preferably about 1 to 1.4 times their diameter, while the distance between the connection bumps 14 in the second bump unit is preferably about 1.6 to 1.7 times their diameter (see, for example, page 5, lines 26 through page 6, line 1). As recited in claims 27 and 29, the bumps of the first and second bump units are preferably formed of solder (see, for example, page 4, lines 17-19).

[Continued on next page]

## VI. ISSUES

The issue is whether claims 20, 22, 24-29 and 31 are obvious over Bond et al., U.S. Patent No. 5,642,261.

## VII. BRIEF DESCRIPTION OF THE REFERENCES

The Bond et al. patent describes a ball grid array (BGA) integrated circuit package that provides a path of high thermal conductivity for an encapsulated integrated circuit chip. The package utilizes a substrate through which an opening has been formed to receive a thermally conductive slug, made of a material such as copper. The integrated circuit chip is mounted to one surface of the slug, and the opposite surface of the slug is exposed at the underside of the substrate. The chip is wire bonded to the substrate and connected in the conventional matter through the substrate to lands on the underside of the substrate outside the periphery of the slug. Solder balls are attached to the underside of the substrate and of the slug in ball-grid-array fashion, for mounting to a circuit board. Upon mounting to the circuit board, a path of high thermal conductivity is formed between the chip and the circuit board, through the slug and the solder balls. According to one of the disclosed embodiments, the slug extends below the underside of the substrate and has a solder mask with larger apertures than those used for the electrical connections to the substrate, so that when solder balls with equivalent volumes are used to connect to the circuit board, broader conductive leads are formed under the slug for enhanced conductivity.

The Katchmar patent, which is mentioned in the Final Office Action but not specifically relied upon, describes a surface mount area-array integrated circuit package consisting of a substrate, a semiconductor die electrically and mechanically connected to the top surface of

package substrate, an area-array of conductive surface mount terminations (e.g., solder balls) electrically and mechanically connected to the bottom of the package substrate and at least one adhesive mass. The adhesive mass is located on the bottom of the package substrate and replaces the conductive terminations in the area where the joint strain energy density is calculated to be the greatest. When mounted on a substrate, the adhesive mass adheres the package to substrate, achieving increased mechanical and electrical reliability.

## VIII. THE REJECTION

In the final Official Action dated October 22, 2003, from which this Appeal is taken, claims 20, 22, 24-29 and 31 stand rejected under 35 U.S.C. §103(a) as obvious over Bond et al., U.S. Patent No. 5,642,261.

## IX. GROUPING OF CLAIMS

The invention is defined within groupings of claims (i) 20, 22 and 24-25, (ii) 26-27, and (iii) 28-29 and 31. Claims 22 and 24-25 stand or fall with their base claim 20, claim 27 stands or falls with its base claim 26, and claim 29 and 31 stand or fall with their base claim 28. Claims 20, 26 and 28 each recite features that form an independent basis for allowance.

## X. ARGUMENT

Appellant respectfully traverses the rejection based on the prior art applied against the claims now pending on appeal. As discussed below, it is respectfully submitted that the Examiner has not met the burden of proof in establishing that the appealed claims are obvious. It is further respectfully submitted that the rejection of the pending claims fails to provide the required factual

basis or even a reasonable rational for the rejection, and fails to apply art that teaches or suggests the claimed invention.

1. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE

The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the examiner. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). It also is incumbent upon the Examiner to provide a basis in fact and/or cogent technical reasoning to support the conclusion that one having ordinary skill in the art would have been motivated to combine references to arrive at a claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). In so doing, the Examiner is required to make the factual determinations set forth in Graham v. John Deere Co. of Kansas City, 383 U.S. 1, 148 USPQ 459 (1966), and to provide a reason why one having ordinary skill in the art would have been led to modify the prior art reference to arrive at the claimed invention. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985). Such a reason must stem from some teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.d 281, 227 USPQ 657 (Fed. Cir. 1985); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir.

1983). Inherency requires certainty, not speculation. In re Rijckaert, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); W. L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); In re Wilding, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). Objective evidence must be relied upon to defeat the patentability of the claimed invention. Ex parte Natale, 11 USPQ2d 1222 (BPAI 1988). Teaching away from the claimed invention by the prior art is a per se demonstration of lack of prima facie obviousness. In re Dow Chemical Co., 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1988), In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987)

Claims 20, 22, 24-29 and 31 stand rejected under 35 U.S.C. §103(a) as obvious over Bond et al., U.S. Patent No. 5,642,261. As discussed below, it is respectfully submitted that the Examiner has not met the burden of proof in establishing the obviousness of the appealed claims.

In the Final Office Action, the Examiner relies on the Bond et al. reference (hereinafter "Bond") to teach the features of the semiconductor device claimed in the present invention. Specifically, the Examiner points to Bond as teaching a semiconductor device 8 (Figures 1-6), comprising a semiconductor substrate 14 having a main surface and a back surface, wherein the back surface has a central area, a distinct intermediate area surrounding the central area and a peripheral area surrounding the intermediate area; a semiconductor chip formed on the main surface; a first bump unit formed of solder bumps 18 disposed a first distance apart from each other, and located in the distinct area beneath a thermally conducted slab 12 in the central area of the back surface, wherein the first bump unit radiates heat from said semiconductor device; a second bump formed of solder bumps 18 disposed a second distance apart from each other located in the peripheral area of the back surface, wherein the second bump unit transmits

signals, wherein the second bump unit is greater in quantity of solder balls than the first bump unit, and the solder balls are spherical in shape. With regard to the claim requirements that the second distance is greater than the first distance, that the second distance is less than a width of the intermediate area, and that the bumps of first (central) bump unit are located sufficiently close to each other that upon the application of heat treatment to the device, they will fuse into a unitary body (claims 20, 22, 24-29), and with respect to the requirement that the first distance is about 1 to 1.4 times the diameter of bumps of the first bump unit and the second distance is about 1.6 to 1.7 times the diameter of the bumps of the second bump unit (claims 31), the Examiner asserts it would have been obvious to one skilled in the art at the time the invention was made to employ a distinct intermediate area between the first and second groups of solder balls, the second distance being less than the width of the intermediate area, and to locate the bumps of the first bump unit so close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit would be fused into us a unitary body, or to make the first distance about 1 to 1.4 times the diameter of the bumps of the first bump unit, and the second distance about 1.6 to 1.7 times the diameter of the bumps of the second bump in the devise by Bond in order to avoid shorting between thermal and signal solder balls, or to melt the thermal solder balls into a unitary body, while applying heat. The Examiner argues that such a modification of Bond would have involved a mere change in the sizes of components or a mere change in the ranges of sizes, and that such changes are generally recognized as being within the level of ordinary skill in the art. The Examiner also argues that the changes in distance and size would have been obvious to one having ordinary skill in the art at the time the invention was made since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or workable ranges involves only routine skill in the art.

The applicant disagrees with the Examiner's assertion that the claimed relationships between the first and second distances, and between the second distance and the width of the intermediate area, are merely the discovery of "the optimum or workable ranges" that involve "only routine skill in the art" that would render the claims obvious to one of ordinary skill. Rather, these features clearly patentably distinguish the independent claims over the teachings of the applied prior art. While, Bond generally discloses the presence of central and peripheral areas of solder bumps, distinguished by their respective thermal and signal transfer functions, it fails to disclose any requirement regarding the respective spacings within or between the bump units. For example, Figures 1, 3, 4 and 6, which show the various embodiments in cross section, do not disclose any consistent pattern of spacing between bumps in the central and peripheral areas. In fact, it appears from the figures that the spacing between bumps is generally the same in both areas.

Further, it is submitted that Bond lacks any disclosure of a distinct intermediate area, which is devoid of bumps and has a width greater than the distance between the bumps in the peripheral area, as the claims require. The scope of the limitation "a distinct intermediate area in which no bumps are disposed," recited in the present claims, should, in this case, be construed with reference to the specification, where a distinct intermediate area having no bumps is shown, for example, in Figures 1-3. See In re Barr, 44 F.2d 588, 170 USPQ 330 (CCPA 1971). In contrast, Bond discloses no such clear gap between the central and peripheral areas. The only general limitation taught by Bond is that the peripheral array of signal bumps must be located outside the dimensional profile of the thermal conductive slug.

In the claimed invention, "the first and second distances are set such that upon application of a heat treatment to the device, the bumps of the first bump unit melt so as to become

connected and fuse to each other as a unitary body and the bumps of the second bump unit melt and remain apart from each other" (claims 26 and 28). In Bond, on the other hand, the relative distances between bumps in the central and peripheral areas are not of principal concern because the degree to which the solder balls spread in the central area, when the device is heated to mount it to a circuit board, is determined by the apertures 83 in solder mask 81 positioned on the bottom of conductive slug 72 (see Figures 5 and 6). Using solder balls in the central and peripheral areas having the same equivalent volume, the result, in the preferred embodiment in Bond, is that the solder leads 80′ in the central area under the slug, after reflowing the solder balls, will have a cross-sectional area that, on average, is approximate twice that of the leads 78′ in the peripheral area (column 7, line 66, through column 8, line 2). Bond fails to teach or suggest in any way that "the bumps of the second bump unit melt so as to become connected and fuse to each other as a unitary body," as presently claimed. Rather, Bond clearly teaches away from the present invention by using a solder mask to keep the central solder leads separate. Hence, it is submitted that the prior art relied upon by the Examiner provides no motivation to modify the prior art to arrive at the claimed invention. The difference between the claimed invention and Bond is not a matter of degree, as the Examiner asserts, but rather one of kind. The Applicant believes that the Examiner has simply not met the burden of establishing a clearly reasoned basis for denying patentability.

2. THE APPLIED REFERENCES FAIL TO SUGGEST THE CLAIMED INVENTION

In determining obviousness, the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed. Hartness Int'l, Inc. v. Simplimatic Eng'g Co., 819 F.2d 1100, 2 USPQ2d 1826 (Fed. Cir. 1987). It is impermissible to pick and choose from any one reference only so much of it as will support a given

position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. In re Wesslau, 353 F.2d 238, 147 USPQ 391 (CCPA 1951). Piecemeal reconstruction of prior art patents is improper, In re Kamm, 452 F.2d 1052, 172 USPQ 298 (CCPA 1972). The Examiner must give adequate consideration to the particular problems and solution addressed by the claimed invention. Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); In re Rothermel, 276 F.2d 393, 125 USPQ 328 (CCPA 1960).

The fact that the prior art could be modified so as to result in the combination defined by the claims does not make the modification obvious unless the prior art suggests the desirability of the modification. In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). The test is what the combined teachings would have suggested to those of ordinary skill in the art. In re Keller, 642 F.2d 413, 208 USPQ 817 (CCPA 1981). Simplicity and hindsight are not proper criteria for resolving obviousness, In re Warner, supra. The proper approach to the issue of obviousness is whether the hypothetical person of ordinary skill in the art, familiar with the references, would have found it obvious to make a structure corresponding to what is claimed. In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). Hindsight obviousness after the invention has been made is not the test. In re Carroll, 601 F2d 1184, 202 USPQ 571 (CCPA 1979). The reference, viewed by itself and not in retrospect, must suggest doing what applicant has done. In re Shaffer, 229 F2d 476, 108 USPQ 326 (CCPA 1956); In re Skoll, 523 F2d 1392, 187 USPQ 481 (CCPA 1975).

The issue is not whether it is within the skill of the artisan to make the proposed modification but, rather, whether a person of ordinary skill in the art, upon consideration of the references, would have found it obvious to do so. The fact that the prior art could be modified so as

to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggests the desirability of the modification. See In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984), In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986), In re Keller, supra. See In re Laskowski, F2d., 10 USPQ2d 1397 (CAFC 1989). References are not properly combinable or modifiable if their intended purpose or function is destroyed by the combination or modification. See In re Gordon, supra.

Obviousness does not require absolute predictability but a reasonable expectation of success is necessary. In re Clinton, 527 F.2d 1226, 188 USPQ 365 (CCPA 1976), Amgen, Inc. v. Chugai Pharmaceutical Co. Ltd., 927 f.2d 1200, 18 USPQ2d 1016 (Fed. Cir. 1991). A prior art suggestion for virtually endless experimentation is not a case of prima facie obviousness. In re Dow Chemical Co., 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1989)

In the Response to Arguments section of the Final Office Action, the Examiner indicates that the rejection of the pending claims is based in part on an alleged "admission" in the Applicant's Request for Reconsideration of September 30, 2003, which immediately preceded the Final Office Action, namely, "that, in this case, a person of ordinary skill in the art could readily determine what spacing, or range of spacings, of the bumps in the first bump unit would be sufficiently close such that the bumps would fuse into a unitary body upon application of the heat treatment."

Relying on the foregoing "admission," the Examiner gives several reasons for the Final rejection. First, the Examiner asserts that the applicant claims a semiconductor device having a plurality of separate solder bumps in a signal peripheral area or in a heat transferring central area, and does not claim a unitary heat transferring body as part of the claimed structure, but merely as a goal, which could be achieved by using the specifics of the claim. The Examiner goes on to

argue that although Katchmar (U.S. Patents No. 6,194,782, referenced in previous Office Actions by the Examiner) discloses the possibility of having a unitary body in a central heat transferring area in a structure substantially similar to one claimed by the applicant, because of the applicant's new admission, the examiner no longer sees the necessity to rely on Katchmar for the rejection of the instant application.

The "admission" highlighted by the Examiner is simply a recognition of an argument made by the Examiner himself in an earlier Office Action in connection with claimed 31, namely, that it would have been an obvious matter of design choice to make the distance between the bumps in the first bump unit about 1 to 1.4 times the diameter of the bumps, since such a change in size is generally recognized as being within the level of ordinary skill in the art. Even if the quoted statement made by the applicant in the Request for Reconsideration may be considered an "admission," it is an admission only to the fact that the appropriate ranges of solder ball spacings to meet the objectives of the claim may be determined without undue experimentation, and are therefore within the level of ordinary skill in the art. However, it is not an admission that the prior art teaches or suggests the important inventive feature defined in claims 26 and 28, namely, that the bumps of the first bump unit are sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body.

As has already been demonstrated, Bond fails to teach or suggests this feature. Bond, in fact, teaches away by disclosing a solder mask that limits the diameter of the connecting leads in the central area and prevents them from fusing, when the solder balls are reflowed to mount the semiconductor device to a printed circuit board. Katchmar, briefly discussed above, discloses in one embodiment (Figure 5), the use of solder balls arranged in close proximity to each other

under the semiconductor chip (die) 18 in the central area. However, Katchmar fails to teach or suggest that the solder balls in this embodiment are melted and fused together to form a unitary body as a result of heat treatment during the mounting process, as claims 26 and 28 require. Katchmar also discloses in another embodiment (Figure 4) the use of a singe central solder mass 26 that bonds during the reflow process to both the solderable pad 32 on the bottom surface 16 of the package substrate 12 and the solderable pad 34 on the top surface 30 of the printed circuit 28. The first-mentioned embodiment is fabricated with solder balls under the central area that retain their individual identity after heat treatment, and the second-mentioned embodiment starts with a single central solder mass that similarly retains its character after heat treatment. There is simply no suggestion in Katchmar to modify the first-mentioned embodiment to replicate the results of the second mentioned embodiment.

The Examiner's second argument is that a method to make a heat transferring solid soldering unitary body coupled to the substrate of the semiconductor device cannot be claimed as part of the structural ("apparatus") patent application, but rather should be an object of another patent application directed the technological methods. The applicant respectfully disagrees. The limitations in claims 26 and 28 to which the Examiner objects, constitute functional limitations, i.e., they defining a feature of the invention by what it does, rather than what it is, such as its specific structure or composition. As indicated in MPEP section 2173.05(g), there is nothing inherently improper with defining some part of an invention in functional terms. Functional language does not, in and of self, render a claim indefinite. The question to be considered, just as with any other claim limitation, is what the limitation fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. As discussed above, it is clear in this case that a person of ordinary skill in the art could readily determine what spacing, or range of

spacings, of the bumps in the first bump unit would be sufficiently close such that the bumps would fuse into a unitary body upon application of the heat treatment.

The Examiner's third argument is that a major problem in making solder ball (bump) connections is to avoid shorting between them during the reflow process. In order to avoid such shorting, it is well-known in the art to manipulate the sizes of the balls and/or the distances between them, as well as using special solder masks or other methods. Therefore, argues the Examiner, manipulating the size of the balls and/or the distances between them in order to achieve such shorting is inherently also known in the art.

Although it may be known that placing solder ball connections too close to each other may result in shorting during reflow, the prior art, as the Examiner acknowledges, teaches away from such practice. Certainly, none of the references the Examiner has cited, such as Bond and Katchmar, teach or suggest positioning solder bumps on an integrated circuit device sufficiently close to each other that upon the application of a heat treatment to the device, the bumps fuse into a unitary body. Contrary to the Examiner's conclusion, it is respectfully submitted that the use of this technique to achieve the benefits of the present invention would not be obvious to one of ordinary skill considering the prior art as a whole. Simply picking one element in hindsight out of the prior art, without considering what the prior art as a whole teaches, does not support an obviousness rejection.

The Examiner's fourth argument is that because all of the data and explanations given by the applicant, either in the specification or in the following communications, about the size of the bumps or different spacings between them in the central and commercial areas, as well as between these areas, is directed to the goals of achieving shorting between the solder balls or avoiding it, the Examiner came to the conclusion that, based on the applicant's new admission, a

person of ordinary skill in the art could readily determine what spacing, or range of spacings, of the bumps in the first bump unit would be sufficiently close such that the bumps would fuse into a unitary body upon application of the heat treatment, and what spacing, or range of spacings, of the bumps in the peripheral units or between the units would be sufficient to avoid shorting upon application of the treatment (i.e., reflowing).

As discussed above, the admission alleged by the Examiner goes only to the fact that the appropriate ranges of solder ball spacings to meet the objectives of the claim may be determined without undue experimentation, and are therefore within the level of ordinary skill in the art. It is not to be construed as an admission that the prior art teaches or suggests the functional limitation recited in claims 26 and 28, namely, that the bumps of the first bump unit are sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body. The Examiner's argument confuses these two issues, assuming that the recited functional limitation is simply a matter of "sizes" and "ranges."

In his fifth argument, the Examiner insists that Bond does teach a distinct heat transferring first bump unit area by describing it as located beneath the conductive slab 12 (Bond column 4, lines 34-37), as opposed to the second, peripheral bump unit.

This argument is not understood. The language of the claims under appeal refers to a "distinct intermediate area in which no bumps are disposed" (emphasis added), between the central area and the peripheral area. There is no issue between the applicant and the Examiner as to whether the Bond reference discloses separate central and peripheral areas; it is on the matter of a distinct intermediate area that there is disagreement.

## CONCLUSION

In summary, it is respectfully submitted that the Examiner has (i) failed to establish a prima facie case for the rejection, (ii) failed to apply art which teaches or suggests, the claimed invention, and (iii) has applied art in a manner inconsistent with its teachings. The applied art does not provide any teaching, or suggestion within its teachings, which would lead to the features or advantages of the instant invention discussed above, and that for at least these reasons the appealed claims patentably define over the art.

Thus, it is submitted that the rejection of claims 20, 22, 24-29 and 31 under 35 U.S.C. §103(a) as obvious over Bond et al., U.S. Patent No. 5,642,261, is in error and reversal is clearly in order and is courteously solicited.

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PGA/rw
Appendix

# APPENDIX

## CLAIMS ON APPEAL

20. A semiconductor device, comprising:

a substrate having a main surface and a back surface,

wherein said back surface has a central area, a distinct intermediate area in which no bumps are disposed, surrounding said central area, and a peripheral area surrounding said intermediate area;

a semiconductor chip disposed on said main surface;

a first bump unit disposed in said central area of said back surface,

wherein said first bump unit includes a plurality of bumps that are disposed a first distance apart from each other, and

wherein said first bump unit radiates heat from said semiconductor device; and

a second bump unit formed in said peripheral area of said back surface,

wherein said second bump unit includes a plurality of bumps that are disposed a second distance apart from each other, said second distance is greater than said first distance, and said second distance is less than a third distance between said central area and said peripheral area, and

wherein said second bump unit transmits signals.

22. The semiconductor device in accordance with Claim 20, wherein a width of said intermediate area of said back surface is greater than said second distance.

24. The semiconductor device in accordance with Claim 22, wherein said plurality of bumps

included in said second bump unit is greater in quantity than said plurality of bumps included in said first bump unit.

25. The semiconductor device in accordance with Claim 24, wherein said plurality of bumps included in said first bump unit and said second bump unit are spherical in shape.

26. A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed on the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other, the second distance being greater than the first distance and less than a third distance between the central area and the peripheral area,

wherein the first and second distances are set such that upon application of a heat treatment to the device, the bumps of the first bump unit melt so as to become connected and fuse to each other as a unitary body and the bumps of the second bump unit melt and remain apart from each other.

27. The semiconductor device according to claim 26, wherein the bumps of the first and second bump units are formed of solder.

28. (Twice Amended) A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, a distinct intermediate area in which no bumps are disposed, surrounding the central area, and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed on the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other sufficient to assure that upon application of a heat treatment to the device causing the bumps of the first and second bump units to melt, the bumps of the second bump unit remain apart from each other, the second distance being greater than the first distance and less than a width of the intermediate area;

wherein the bumps of the first bump unit are sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body.

29. The semiconductor device according to claim 26, wherein the bumps of the first and second bump units are formed of solder.

31. The semiconductor device according to claim 25, wherein the first distance is about 1 to 1.4 times the diameter of the bumps of the first bump unit, and the second distance is about 1.6 to 1.7 times the diameter of the bumps of the second bump unit.